ABSTRACT OF THE DISCLOSURE

A video decoder reproduces an MP@ML/MPEG-2 video bit stream at an arbitrary speed. When a slice decoder control circuit receives parameters, the slice decoder control circuit sequentially supplies parameters of a picture layer and a write pointer associated with a first slice to a first slice decoder, the parameters of the picture layer and a write pointer associated with a second slice to a second slice decoder, the parameters of the picture layer and a write pointer associated with a third slice to a third slice decoder, so that the slices are decoded by the respective slice decoders. On the basis of signals indicating completion of decoding, received from the first to third slice decoders, the slice decoder control circuit gives commands the first to third slice decoders to decode particular slices.